



XC95144XV High-Performance CPLD

DS051 (v2.2) August 27, 2001

Advance Product Specification

Features

- 144 macrocells with 3,200 usable gates
- Available in small footprint packages
 - 100-pin TQFP (81 user I/O pins)
 - 144-pin TQFP (117 user I/O pins)
 - 144-pin CSP (117 user I/O pins)
- Optimized for high-performance 2.5V systems
 - Low power operation
 - Multi-voltage operation
- Advanced system features
 - In-system programmable
 - Two separate output banks
 - Superior pin-locking and routability with FastCONNECT II™ switch matrix
 - Extra wide 54-input Function Blocks
 - Up to 90 product-terms per macrocell with individual product-term allocation
 - Local clock inversion with three global and one product-term clocks
 - Individual output enable per output pin
 - Input hysteresis on all user and boundary-scan pin inputs
 - Bus-hold circuitry on all user pin inputs
 - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
 - Endurance exceeding 10,000 program/erase cycles
 - 20 year data retention
 - ESD protection exceeding 2,000V

Description

The XC95144XV is a 2.5V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of eight 54V18 Function Blocks, providing 3,200 usable gates with propagation delays of 4 ns.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XV device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC} , the following equation may be used:

$$I_{CC} \text{ (mA)} = MC_{HP}(0.36) + MC_{LP}(0.23) + MC(0.005 \text{ mA/MHz}) f$$

Where:

MC_{HP} = Macrocells in high-performance (default) mode

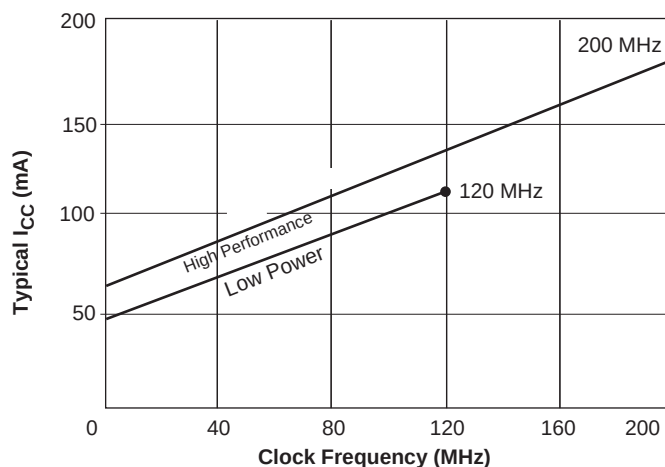
MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

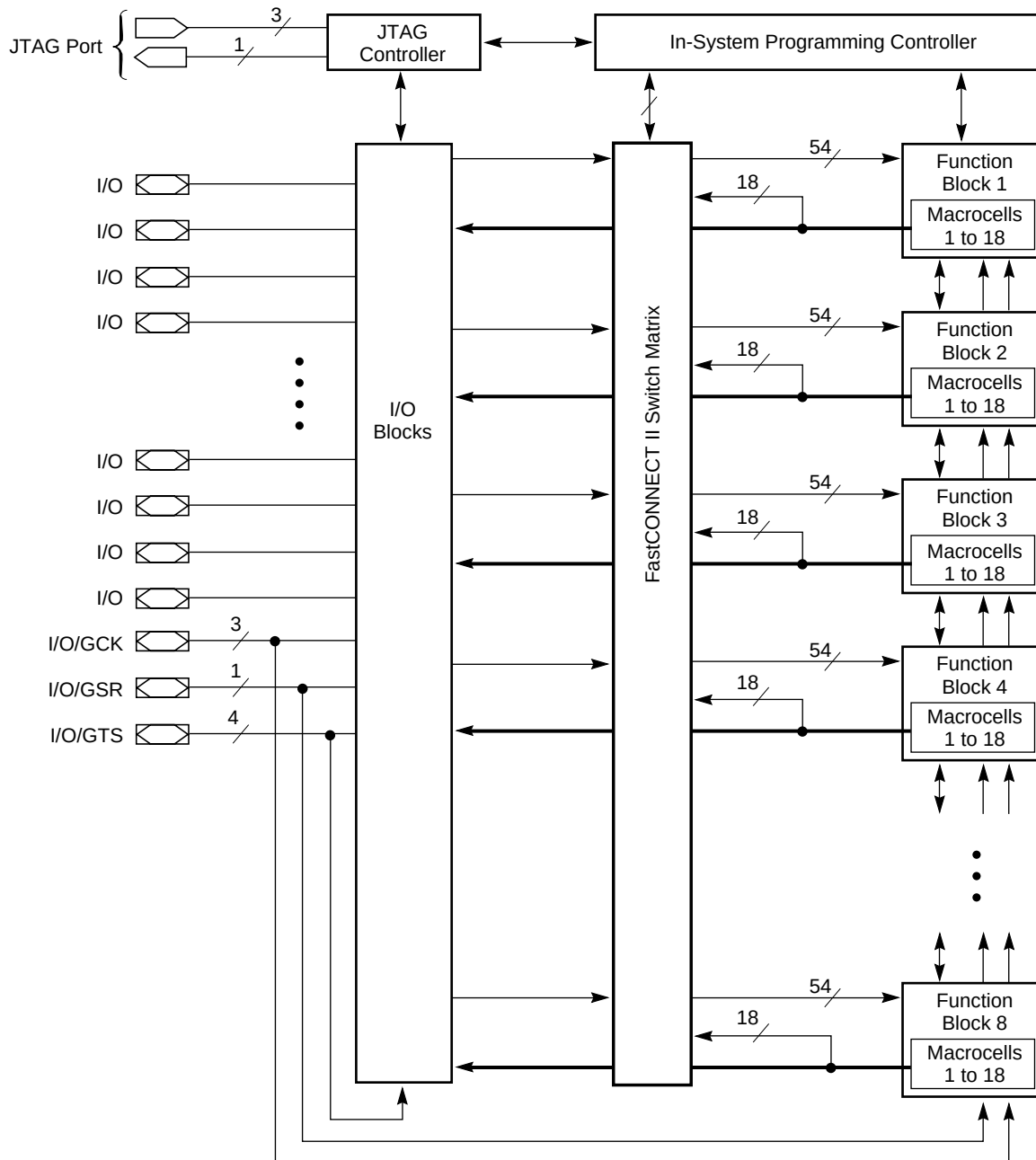
This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual I_{CC} value varies with the design application and should be verified during normal system operation.

Figure 1 shows the above estimation in a graphical form.



DS051_01_012501

Figure 1: Typical I_{CC} vs. Frequency for XC95144XV



DS051_02_041000

Figure 2: XC95144XV Architecture

Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to 2.7	V
V_{CCIO}	Supply voltage for output drivers	–0.5 to 3.6	V
V_{IN}	Input voltage relative to GND ⁽¹⁾	–0.5 to 3.6	V
V_{TS}	Voltage applied to 3-state output ⁽¹⁾	–0.5 to 3.6	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C
T_J	Junction temperature	+150	°C

Notes:

1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0V or overshoot to +3.6V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffers	Commercial $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	2.37	2.62	V
		Industrial $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	2.37	2.62	
V_{CCIO}	Supply voltage for output drivers for 3.3V operation		3.13	3.46	V
	Supply voltage for output drivers for 2.5V operation		2.37	2.62	V
	Supply voltage for output drivers for 1.8V operation		1.71	1.89	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{IH}	High-level input voltage		1.7	3.6	V
V_O	Output voltage		0	V_{CCIO}	V

Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
T_{DR}	Data retention	20	-	Years
N_{PE}	Program/Erase cycles (endurance)	10,000	-	Cycles
V_{ESD}	Electrostatic Discharge (ESD)	2,000	-	Volts

DC Characteristics (Over Recommended Operating Conditions)

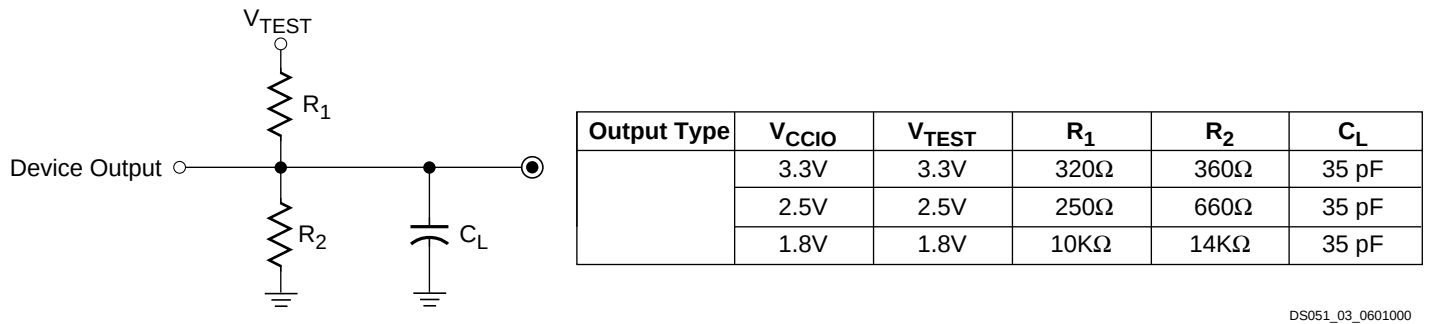
Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 3.3V outputs	$I_{OH} = -4.0 \text{ mA}$	2.4	-	V
	Output high voltage for 2.5V outputs	$I_{OH} = -1.0 \text{ mA}$	2.0	-	V
	Output high voltage for 1.8V outputs	$I_{OH} = -100 \mu\text{A}$	90% V_{CCIO}	-	V
V_{OL}	Output low voltage for 3.3V outputs	$I_{OL} = 8.0 \text{ mA}$	-	0.4	V
	Output low voltage for 2.5V outputs	$I_{OL} = 1.0 \text{ mA}$	-	0.4	V
	Output low voltage for 1.8V outputs	$I_{OL} = 100 \mu\text{A}$	-	0.4	V
I_{IL}	Input leakage low current	$V_{CC} = 2.62\text{V}$ $V_{CCIO} = 3.6\text{V}$ $V_{IN} = \text{GND or } 3.6\text{V}$	-	10	μA
I_{IH}	Input leakage high current	$V_{CC} = 2.62\text{V}$ $V_{CCIO} = 3.6\text{V}$ $V_{IN} = \text{GND or } 3.6\text{V}$	-	10	μA
C_{IN}	I/O capacitance	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$	-	10	pF
I_{CC}	Operating Supply Current (low power mode, active)	$V_I = \text{GND, No load}$ $f = 1.0 \text{ MHz}$	29		mA

AC Characteristics

Symbol	Parameter	XC95144XV-4		XC95144XV-5		XC95144XV-7		Units
		Min	Max	Min	Max	Min	Max	
T_{PD}	I/O to output valid	-	4.0	-	5.0	-	7.5	ns
T_{SU}	I/O setup time before GCK	2.8	-	3.5	-	4.8	-	ns
T_H	I/O hold time after GCK	0	-	0	-	0	-	ns
T_{CO}	GCK to output valid	-	2.8	-	3.5	-	4.5	ns
f_{SYSTEM}	Multiple FB internal operating frequency	-	250.0	-	222.2	-	125.0	MHz
T_{PSU}	I/O setup time before p-term clock input	0.8	-	1.0	-	1.6	-	ns
T_{PH}	I/O hold time after p-term clock input	2.0	-	2.5	-	3.2	-	ns
T_{PCO}	P-term clock output valid	-	4.8	-	6.0	-	7.7	ns
T_{OE}	GTS to output valid	-	3.2	-	4.0	-	5.0	ns
T_{OD}	GTS to output disable	-	3.2	-	4.0	-	5.0	ns
T_{POE}	Product term OE to output enabled	-	5.6	-	7.0	-	9.5	ns
T_{POD}	Product term OE to output disabled	-	5.6	-	7.0	-	9.5	ns
T_{AO}	GSR to output valid	-	7.9	-	10.0	-	12.0	ns
T_{PAO}	P-term S/R to output valid	-	8.5	-	10.7	-	12.6	ns
T_{WLH}	GCK pulse width (High or Low)	2.0	-	2.2	-	4.0	-	ns
T_{PLH}	P-term clock pulse width (High or Low)	5.0	-	5.0	-	6.5	-	ns
Advance Information				Preliminary Information				

Notes:

1. Please contact Xilinx for up-to-date information on advance specifications.



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Figure 3: AC Load Circuit

Internal Timing Parameters

Symbol	Parameter	XC95144XV-4		XC95144XV-5		XC95144XV-7		Units
		Min	Max	Min	Max	Min	Max	
Buffer Delays								
T _{IN}	Input buffer delay	-	1.6	-	2.0	-	2.3	ns
T _{GCK}	GCK buffer delay	-	1.0	-	1.2	-	1.5	ns
T _{GSR}	GSR buffer delay	-	1.6	-	2.0	-	3.1	ns
T _{GTS}	GTS buffer delay	-	3.2	-	4.0	-	5.0	ns
T _{OUT}	Output buffer delay	-	1.6	-	2.1	-	2.5	ns
T _{EN}	Output buffer enable/disable delay	-	0	-	0	-	0	ns
Product Term Control Delays								
T _{PTCK}	Product term clock delay	-	1.4	-	1.7	-	2.4	ns
T _{PTSR}	Product term set/reset delay	-	0.6	-	0.7	-	1.4	ns
T _{PTTS}	Product term 3-state delay	-	4.0	-	5.0	-	7.2	ns
Internal Register and Combinatorial Delays								
T _{PDI}	Combinatorial logic propagation delay	-	0.2	-	0.2	-	1.3	ns
T _{SUI}	Register setup time	1.6	-	2.0	-	2.6	-	ns
T _{HI}	Register hold time	1.2	-	1.5	-	2.2	-	ns
T _{ECSU}	Register clock enable setup time	1.6	-	2.0	-	2.6	-	ns
T _{ECHO}	Register clock enable hold time	1.2	-	1.5	-	2.2	-	ns
T _{COI}	Register clock to output valid time	-	0.2	-	0.2	-	0.5	ns
T _{AOI}	Register async. S/R to output delay	-	4.7	-	5.9	-	6.4	ns
T _{RAI}	Register async. S/R recover before clock	4.0		5.0		7.5		ns
T _{LOGI}	Internal logic delay	-	0.6	-	0.7	-	1.4	ns
T _{LOGILP}	Internal low power logic delay	-	5.6	-	5.7	-	6.4	ns
Feedback Delays								
T _F	FastCONNECT II™ feedback delay	-	1.6	-	1.6	-	3.5	ns
Time Adders								
T _{PTA}	Incremental product term allocator delay	-	0.6	-	0.7	-	0.8	ns
T _{PTA2}	Adjacent macrocell p-term allocator delay	-	0.2	-	0.3	-	0.3	ns
T _{SLEW}	Slew-rate limited delay	-	3.0	-	3.0	-	4.0	ns
		Advance Information		Preliminary Information				

Notes:

- Please contact Xilinx for up-to-date information on advance specifications.

XC95144XV I/O Pins

Function Block	Macro-cell	TQ100	TQ144	CS144	BScan Order	Bank	Function Block	Macro-cell	TQ100	TQ144	CS144	BScan Order	Bank
1	1	-	23	H3	429	1	3	1	-	39	M3	321	1
1	2	11	16	F1	426	1	3	2	23 ⁽¹⁾	32 ⁽¹⁾	L1 ⁽¹⁾	318	1
1	3	12	17	G2	423	1	3	3	-	41	K4	315	1
1	4	-	25	J1	420	1	3	4	-	44	N4	312	1
1	5	13	19	G3	417	1	3	5	24	33	L2	309	1
1	6	14	20	G4	414	1	3	6	25	34	L3	306	1
1	7	-	-	-	411	-	3	7	-	46	L5	303	1
1	8	15	21	H1	408	1	3	8	27 ⁽¹⁾	38 ⁽¹⁾	N2 ⁽¹⁾	300	1
1	9	16	22	H2	405	1	3	9	28	40	N3	297	1
1	10	-	31	K3	402	1	3	10	-	48	N5	294	1
1	11	17	24	H4	399	1	3	11	29	43	M4	291	1
1	12	18	26	J2	396	1	3	12	30	45	K5	288	1
1	13	-	-	-	393	-	3	13	-	-	-	285	-
1	14	19	27	J3	390	1	3	14	32	49	K6	282	1
1	15	20	28	J4	387	1	3	15	33	50	L6	279	1
1	16	-	35	M1	384	1	3	16	-	-	-	276	-
1	17	22 ⁽¹⁾	30 ⁽¹⁾	K2 ⁽¹⁾	381	1	3	17	34	51	M6	273	1
1	18	-	-	-	378	-	3	18	-	-	-	270	-
2	1	-	142	C3	375	2	4	1	-	118	C9	267	2
2	2	99 ⁽¹⁾	143 ⁽¹⁾	A2 ⁽¹⁾	372	2	4	2	87	126	A7	264	2
2	3	-	-	-	369	-	4	3	-	133	A5	261	2
2	4	-	4	C1	366	2	4	4	-	-	-	258	-
2	5	1 ⁽¹⁾	2 ⁽¹⁾	B1 ⁽¹⁾	363	2	4	5	89	128	D7	255	2
2	6	2 ⁽¹⁾	3 ⁽¹⁾	C2 ⁽¹⁾	360	2	4	6	90	129	A6	252	2
2	7	-	-	-	357	-	4	7	-	-	-	249	-
2	8	3 ⁽¹⁾	5 ⁽¹⁾	D4 ⁽¹⁾	354	2	4	8	91	130	B6	246	2
2	9	4 ⁽¹⁾	6 ⁽¹⁾	D3 ⁽¹⁾	351	2	4	9	92	131	C6	243	2
2	10	-	7	D2	348	2	4	10	-	135	C5	240	2
2	11	6	9	E4	345	2	4	11	93	132	D6	237	2
2	12	7	10	E3	342	2	4	12	94	134	B5	234	2
2	13	-	12	E1	339	2	4	13	-	137	A4	231	2
2	14	8	11	E2	336	2	4	14	95	136	D5	228	2
2	15	9	13	F4	333	2	4	15	96	138	B4	225	2
2	16	-	14	F3	330	2	4	16	-	139	C4	222	2
2	17	10	15	F2	327	2	4	17	97	140	A3	219	2
2	18	-	-	-	324	-	4	18	-	-	-	216	-

Notes:

1. Global control pin.

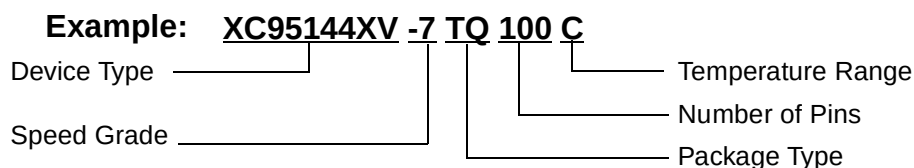
Function Block	Macro-cell	TQ100	TQ144	CS144	BScan Order	Bank
5	1	-	-	-	213	-
5	2	35	52	N6	210	1
5	3	-	59	L8	207	1
5	4	-	-	-	204	-
5	5	36	53	M7	201	1
5	6	37	54	N7	198	1
5	7	-	66	M10	195	1
5	8	39	56	K7	192	1
5	9	40	57	N8	189	1
5	10	-	68	N11	186	1
5	11	41	58	M8	183	1
5	12	42	60	K8	180	1
5	13	-	70	L11	177	1
5	14	43	61	N9	174	1
5	15	46	64	K9	171	1
5	16	-	-	-	168	-
5	17	49	69	M11	165	1
5	18	-	-	-	162	-
6	1	-	-	-	159	-
6	2	74	106	C11	156	2
6	3	-	-	-	153	-
6	4	-	111	B11	150	2
6	5	76	110	A12	147	2
6	6	77	112	A11	144	2
6	7	-	-	-	141	-
6	8	78	113	D10	138	2
6	9	79	116	A10	135	2
6	10	-	115	B10	132	2
6	11	80	119	B9	129	2
6	12	81	120	A9	126	2
6	13	-	-	-	123	-
6	14	82	121	D8	120	2
6	15	85	124	A8	117	2
6	16	-	117	D9	114	2
6	17	86	125	B7	111	2
6	18	-	-	-	108	-

Function Block	Macro-cell	TQ100	TQ144	CS144	BScan Order	Bank
7	1	-	-	-	105	-
7	2	50	71	N12	102	1
7	3	-	75	L12	99	1
7	4	-	-	-	96	-
7	5	52	74	M13	93	1
7	6	53	76	L13	90	1
7	7	-	77	K10	87	1
7	8	54	78	K11	84	1
7	9	55	80	K13	81	1
7	10	-	79	K12	78	1
7	11	56	82	J11	75	1
7	12	58	85	H10	72	1
7	13	-	81	J10	69	1
7	14	59	86	H11	66	1
7	15	60	87	H12	63	1
7	16	-	83	J12	60	1
7	17	61	88	H13	57	1
7	18	-	-	-	54	-
8	1	-	-	-	51	-
8	2	63	91	G11	48	2
8	3	-	95	F11	45	2
8	4	-	97	E13	42	2
8	5	64	92	G10	39	2
8	6	65	93	F13	36	2
8	7	-	-	-	33	-
8	8	66	94	F12	30	2
8	9	67	96	F10	27	2
8	10	-	101	D13	24	2
8	11	68	98	E12	21	2
8	12	70	100	E10	18	2
8	13	-	103	D11	15	2
8	14	71	102	D12	12	2
8	15	72	104	C13	9	2
8	16	-	107	B13	6	2
8	17	73	105	C12	3	2
8	18	-	-	-	0	-

XC95144XV Global, JTAG and Power Pins

Pin Type	TQ100	TQ144	CS144
I/O/GCK1	22	30	K2
I/O/GCK2	23	32	L1
I/O/GCK3	27	38	N2
I/O/GTS1	3	5	D4
I/O/GTS2	4	6	D3
I/O/GTS3	1	2	B1
I/O/GTS4	2	3	C2
I/O/GSR	99	143	A2
TCK	48	67	L10
TDI	45	63	L9
TDO	83	122	C8
TMS	47	65	N10
V _{CCINT} 2.5V	5, 57, 98	8, 42, 84, 141	B3, D1, J13, L4
V _{CCIO1}	26, 38, 51	37, 55, 73	L7, N1, N13
V _{CCIO2}	88	1, 109, 127	A1, A13, C7
GND	21, 31, 44, 62, 69, 75, 84, 100	18, 29, 36, 47, 62, 72, 89, 90, 99, 108, 114, 123, 144	B2, B8, B12, C10, E11, G1, G12, G13, K1, M2, M5, M9, M12
No Connects	-	-	-

Ordering Information



Device Ordering Options

Speed		Package		Temperature	
-7	7.5 ns pin-to-pin delay	TQ100	100-pin Thin Quad Flat Pack (TQFP)	C = Commercial	$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$
-5	5 ns pin-to-pin delay	TQ144	144-pin Thin Quad Flat Pack (TQFP)	I = Industrial	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$
-4	4 ns pin-to-pin delay	CS144	144-ball Chip Scale Package (CSP)		

Component Availability

Pins		100	144	144
Type		Plastic TQFP	Plastic TQFP	Plastic CSP
Code		TQ100	TQ144	CS144
XC95144XV	-7	C, I	C, I	C
	-5	(C)	(C)	(C)
	-4	(C)	(C)	-

Notes:

1. C = Commercial ($T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$); I = Industrial ($T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$).
2. () Parenthesis indicate future planned products. Please contact Xilinx for up-to-date information.

Revision History

The following table shows the revision history for this document..

Date	Version	Revision
06/28/00	1.0	Initial Xilinx release. Advance information specification.
01/25/01	2.0	Added -4 performance specifications. Updated I_{CC} vs. Frequency Figure 1 .
05/15/01	2.1	Updated I_{CC} formula, Recommended Operation Conditions, -4 and -5 AC Characteristics and Internal Timing Parameters
08/27/01	2.2	Changed V_{CCIO} 3.3V from 3.13 to 3.0 (min), 3.46 to 3.60 (max); DC characteristics: I_{IL} - added "low" current, I_{IH} - changed to "Input leakage high current"; Internal Timing: -5 T_{AOI} from 6.5 to 5.9.